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## Inventor Name Search Result

Your Search was:

Last Name = LEE

First Name = SANG-HYUN

provisional

Application#	Patent#	Status	Date Filed	Title	Inventor Name 38
<u>60622698</u>	Not Issued	020	10/28/2004	METHOD FOR READING BCA CODE WITHOUT FG (FREQUENCY GENERATOR)	LEE, SANG-HYUN
<u>60590710</u>	Not Issued	020	07/22/2004	DIVIDE-BY-16.5 FREQUENCY DIVIDER WITH CASCADED DIVIDE-BY-3 AND DIVIDE-BY-5.5 DIVIDERS AND DEVICES INCLUDING SAME	LEE, SANG-HYUN
<u>60416017</u>	Not Issued	159	10/04/2002	2.5-10GBPS CMOS TRANSCEIVER WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	LEE, SANG-HYUN
<u>60229369</u>	Not Issued	159	08/30/2000	DATA RECOVERY USING DATA EYE TRACKING	LEE, SANG-HYUN
<u>29122719</u>	D442175	150	05/03/2000	CASE FOR A PERSONAL COMPUTER	LEE, SANG-HYUN
<u>11107846</u>	Not Issued	020	04/18/2005	FIELD EMISSION DEVICE (FED)	LEE, SANG-HYUN
<u>11105922</u>	Not Issued	030	04/13/2005	DECODING APPARATUS FOR LOW-DENSITY PARITY-CHECK CODES USING SEQUENTIAL DECODING, AND METHOD THEREOF	LEE, SANG-HYUN
<u>11073246</u>	Not Issued	030	03/04/2005	TRANSISTORS OF SEMICONDUCTOR DEVICE HAVING CHANNEL REGION IN A CHANNEL-PORTION HOLE AND METHODS OF FORMING THE SAME	LEE, SANG-HYUN
<u>11066854</u>	Not Issued	020	02/24/2005	METHOD FOR FORMING ELECTRON EMISSION SOURCE FOR ELECTRON EMISSION DEVICE AND ELECTRON EMISSION DEVICE USING THE SAME	LEE, SANG-HYUN
<u>11056995</u>	Not Issued	019	02/11/2005	PHASE LOCK LOOP WITH COARSE CONTROL LOOP	LEE, SANG-HYUN

				HAVING FREQUENCY LOCK DETECTOR AND DEVICE INCLUDING SAME	
<u>11051834</u>	Not Issued	020	02/04/2005	RECESSED-TYPE FIELD EFFECT TRANSISTOR WITH REDUCED BODY EFFECT ✓	LEE, SANG-HYUN
<u>11048809</u>	Not Issued	030	02/03/2005	METHOD OF MANUFACTURING FIELD EMITTER ✓	LEE, SANG-HYUN
<u>11022056</u>	Not Issued	019	12/23/2004	RECESS TYPE MOS TRANSISTOR AND METHOD OF MANUFACTURING SAME ✓	LEE, SANG-HYUN
<u>11021349</u>	Not Issued	030	12/23/2004	ASYMMETRIC MOS TRANSISTOR WITH TRENCH-TYPE GATE ✓	LEE, SANG-HYUN
<u>11000290</u>	Not Issued	020	11/29/2004	APPARATUS AND METHOD FOR ERASURE DETECTION AND SOFT-DECISION DECODING IN CELLULAR SYSTEM RECEIVER ✓	LEE, SANG-HYUN
<u>10964122</u>	Not Issued	020	10/12/2004	APPARATUS FOR ENCODING AND DECODING OF LOW-DENSITY PARITY-CHECK CODES, AND METHOD THEREOF ✓	LEE, SANG-HYUN
<u>10912055</u>	Not Issued	020	08/06/2004	LASER DIODE DRIVING CIRCUIT AND LASER DIODE CONTROLLING APPARATUS INCLUDING THE LASER DIODE DRIVING CIRCUIT ✓	LEE, SANG-HYUN
<u>10896169</u>	Not Issued	020	07/22/2004	GENE ENCODING CYSTEINE PROTEASE AND ITS PROMOTER WHICH ARE EXPRESSED SPECIFICALLY IN RICE ANTHOR, A METHOD FOR PRODUCING MALE STERILE RICE BY SUPPRESSING EXPRESSION OF THE GENE ✓	LEE, SANG-HYUN
<u>10845393</u>	Not Issued	030	05/12/2004	COVER REPLACEMENT ASSEMBLY FOR A MOBILE COMMUNICATION TERMINAL ✓	LEE, SANG-HYUN
<u>10740573</u>	Not Issued	030	12/22/2003	MONOLITHIC INK-JET PRINthead AND METHOD FOR MANUFACTURING THE SAME ✓	LEE, SANG-HYUN
<u>10723528</u>	Not Issued	030	11/25/2003	ADAPTIVE TRANSMISSION AND RECEIVING METHOD AND DEVICE IN WIRELESS COMMUNICATION SYSTEM WITH MULTIPLE ANTENNAS ✓	LEE, SANG-HYUN
<u>10696897</u>	Not Issued	030	10/29/2003	SIMPLIFIED MESSAGE-PASSING DECODER FOR LOW-DENSITY PARITY-CHECK CODES ✓	LEE, SANG-HYUN
<u>10688079</u>	<u>6838341</u>	150	10/16/2003	METHOD FOR FABRICATING	LEE, SANG-HYUN

				SEMICONDUCTOR DEVICE WITH SELF-ALIGNED STORAGE NODE ✓	
<u>10665085</u>	Not Issued	020	09/17/2003	HYBRID MULTI-USER INTERFERENCE CANCELLATION METHOD AND DEVICE USING CLUSTERING ALGORITHM BASED ON DYNAMIC PROGRAMMING ✓	LEE, SANG-HYUN
<u>10642259</u>	Not Issued	030	08/15/2003	DATA SAMPLING METHOD AND APPARATUS WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION ✓	LEE, SANG-HYUN
<u>10606822</u>	Not Issued	020	06/26/2003	DIGITAL FILTER FOR SOFTWARE-DEFINED RADIO SYSTEM, DIGITAL INTERMEDIATE FREQUENCY SIGNAL PROCESSING APPARATUS HAVING THE DIGITAL FILTER, AND METHOD THEREOF ✓	LEE, SANG-HYUN
<u>10334352</u>	Not Issued	040	12/31/2002	METHOD AND DEVICE FOR PERFORMING SOFT DECISION DECODING ON REED-MULLER CODES USING DECISION BY MAJORITY ✓	LEE, SANG-HYUN
<u>10278991</u>	<u>6692112</u>	150	10/24/2002	MONOLITHIC INK-JET PRINthead ✓	LEE, SANG-HYUN
<u>09943029</u>	Not Issued	071	08/29/2001	DATA RECOVERY USING DATA EYE TRACKING	LEE, SANG-HYUN
<u>09376762</u>	<u>6215149</u>	150	08/17/1999	SEMICONDUCTOR DEVICE HAVING A TRENCH TYPE GATE AND A FABRICATION METHOD THEREFOR ✓	LEE, SANG-HYUN
<u>09332732</u>	Not Issued	160	06/14/1999	POWER DEVICE AND METHOD OF MANUFACTURING THE SAME ✓	LEE, SANG-HYUN
<u>09299739</u>	<u>6473664</u>	150	04/27/1999	MANUFACTURING PROCESS AUTOMATION SYSTEM USING A FILE SERVER AND ITS CONTROL METHOD ✓	LEE, SANG-HYUN
<u>08956105</u>	<u>5940336</u>	150	10/24/1997	REFERENCE CLOCK GENERATING CIRCUIT IN MEMORY TO BE ASYNCHRONOUSLY PRECHARGED AND ACTIVATED ✓	LEE, SANG-HYUN
<u>08903876</u>	<u>5825693</u>	150	07/31/1997	WRITE CONTROL CIRCUIT FOR SEMICONDUCTOR MEMORY ✓	LEE, SANG-HYUN

<u>08901627</u>	<u>5883846</u>	150	07/28/1997	LATCH TYPE SENSE AMPLIFIER HAVING A NEGATIVE FEEDBACK DEVICE	LEE, SANG-HYUN
<u>07806938</u>	<u>D346161</u>	150	12/11/1991	KEYBOARD FOR A COMPUTER ✓	LEE, SANG-HYUN
<u>07806923</u>	<u>D346588</u>	150	12/11/1991	COMPUTER ✓	LEE, SANG-HYUN
<u>07806922</u>	<u>D346371</u>	150	12/11/1991	DISPLAY FOR COMPUTER ✓	LEE, SANG-HYUN

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LEE	SANG-HYUN	<input type="button" value="Search"/>

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## Inventor Name Search Result

Your Search was:

Last Name = JEONG

First Name = DEOG-KYOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name 50
<u>60378572</u>	Not Issued	159	05/06/2002	IP ADDRESS LOOKUP SCHEME	JEONG, DEOG-KYOON
<u>60378524</u>	Not Issued	159	05/06/2002	PRIORITY QUEUE FOR HIGH-SPEED PACKET SWITCHES	JEONG, DEOG-KYOON
<u>60378523</u>	Not Issued	159	05/06/2002	SCHEDULER FOR MULTIPLANE CROSSBAR SWITCHES	JEONG, DEOG-KYOON
<u>60230589</u>	Not Issued	159	09/05/2000	OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION	JEONG, DEOG-KYOON
<u>60229369</u>	Not Issued	159	08/30/2000	DATA RECOVERY USING DATA EYE TRACKING	JEONG, DEOG-KYOON
<u>60187370</u>	Not Issued	159	03/06/2000	METHOD AND APPARATUS FOR SERIAL INTERFACE FOR STORAGE DEVICE	JEONG, DEOG-KYOON
<u>60176416</u>	Not Issued	159	01/14/2000	BAUD-RATE TIMING RECOVERY	JEONG, DEOG-KYOON
<u>60164874</u>	Not Issued	159	11/12/1999	RECEIVER	JEONG, DEOG-KYOON
<u>60136640</u>	Not Issued	159	05/27/1999	UNLIMITED FREQUENCY RANGE DELAY-LOCKED LOOP CIRCUIT	JEONG, DEOG-KYOON
<u>60071879</u>	Not Issued	159	01/20/1998	1.25GBAUD CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABIT ETHERNET PHY CHIP	JEONG, DEOG-KYOON
<u>60071805</u>	Not Issued	159	01/20/1998	SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS THROUGH SPREAD SPECTRUM PHASE MODULATION	JEONG, DEOG-KYOON
<u>60058042</u>	Not Issued	159	09/04/1997	POWER SAVING METHODS FOR COLUMN DRIVERS	JEONG, DEOG-KYOON
<u>60058041</u>	Not Issued	159	09/04/1997	DATA DRIVING WITH REDUCED EMI	JEONG, DEOG-KYOON
<u>60058040</u>	Not Issued	159	09/04/1997	DATA RECOVERY SCHEME FOR OVERSAMPLED SYSTEMS	JEONG, DEOG-KYOON
<u>11056995</u>	Not	019	02/11/2005	PHASE LOCK LOOP WITH COARSE	JEONG, DEOG-

	Issued			CONTROL LOOP HAVING FREQUENCY LOCK DETECTOR AND DEVICE INCLUDING SAME	KYOON
<u>10652721</u>	Not Issued	160	08/29/2003	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO	JEONG, DEOG- KYOON
<u>10651500</u>	Not Issued	030	08/29/2003	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO	JEONG, DEOG- KYOON
<u>10642259</u>	Not Issued	030	08/15/2003	DATA SAMPLING METHOD AND APPARATUS WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION	JEONG, DEOG- KYOON
<u>10613442</u>	<u>6888417</u>	150	07/03/2003	VOLTAGE CONTROLLED OSCILLATOR	JEONG, DEOG- KYOON
<u>10612840</u>	Not Issued	030	07/03/2003	TRACKED 3X OVERSAMPLING RECEIVER	JEONG, DEOG- KYOON
<u>10403477</u>	<u>6819166</u>	150	03/31/2003	CONTINUOUS-TIME, LOW- FREQUENCY-GAIN/HIGH- FREQUENCY-BOOSTING JOINT ADAPTATION EQUALIZER AND METHOD	JEONG, DEOG- KYOON
<u>10113600</u>	<u>6538498</u>	150	04/02/2002	GM-C TUNING CIRCUIT WITH FILTER CONFIGURATION	JEONG, DEOG- KYOON
<u>10053461</u>	Not Issued	041	11/07/2001	METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS	JEONG, DEOG- KYOON
<u>10045625</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS	JEONG, DEOG- KYOON
<u>10045606</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR DYNAMIC SEGMENTATION OF COMMUNICATIONS PACKETS	JEONG, DEOG- KYOON
<u>10045601</u>	Not Issued	061	11/07/2001	MULTISECTION MEMORY BANK SYSTEM	JEONG, DEOG- KYOON
<u>10045393</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS	JEONG, DEOG- KYOON
<u>10045348</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR ASYMMETRIC PACKET ORDERING BETWEEN COMMUNICATIONS DEVICES	JEONG, DEOG- KYOON
<u>10045297</u>	Not Issued	061	11/07/2001	COMMUNICATIONS ARCHITECTURE FOR MEMORY- BASED DEVICES	JEONG, DEOG- KYOON

<u>10035911</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS ✓	JEONG, DEOG-KYOON
<u>09766503</u>	Not Issued	160	01/18/2001	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION ✓	JEONG, DEOG-KYOON
<u>09759624</u>	<u>6891910</u>	150	01/12/2001	BAUD-RATE TIMING RECOVERY ✓	JEONG, DEOG-KYOON
<u>09709637</u>	<u>6483355</u>	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME ✓	JEONG, DEOG-KYOON
<u>09574571</u>	<u>6326826</u>	150	05/17/2000	WIDE FREQUENCY-RANGE DELAY-LOCKED LOOP CIRCUIT ✓	JEONG, DEOG-KYOON
<u>09393849</u>	<u>6738417</u>	150	09/09/1999	METHOD AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN A DIGITAL DISPLAY AND A COMPUTER ✓	JEONG, DEOG-KYOON
<u>09298369</u>	<u>6374361</u>	150	04/22/1999	SKEW-INSENSITIVE LOW VOLTAGE DIFFERENTIAL RECEIVER ✓	JEONG, DEOG-KYOON
<u>09234619</u>	<u>6560290</u>	150	01/20/1999	CMOS DRIVER AND ON-CHIP TERMINATION FOR GIGABAUD SPEED DATA COMMUNICATION ✓	JEONG, DEOG-KYOON
<u>09007707</u>	<u>5969552</u>	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP ✓	JEONG, DEOG-KYOON
<u>08815486</u>	<u>6157360</u>	150	03/11/1997	SYSTEM AND METHOD FOR DRIVING COLUMNS OF AN ACTIVE MATRIX DISPLAY ✓	JEONG, DEOG-KYOON
<u>08664136</u>	<u>5835498</u>	150	06/14/1996	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK ✓	JEONG, DEOG-KYOON
<u>08631420</u>	<u>5815041</u>	150	04/12/1996	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE ✓	JEONG, DEOG-KYOON
<u>08581135</u>	<u>5802103</u>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION ✓	JEONG, DEOG-KYOON
<u>08580914</u>	<u>5712585</u>	150	12/29/1995	A SYSTEM FOR DISTRIBRITING CLOCK SIGNALS ✓	JEONG, DEOG-KYOON
<u>08580700</u>	<u>5675584</u>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION ✓	JEONG, DEOG-KYOON
<u>08580571</u>	<u>5587709</u>	150	12/29/1995	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION ✓	JEONG, DEOG-KYOON
<u>08580569</u>	<u>5705947</u>	150	12/29/1995	CLOCK GENERATOR ✓	JEONG, DEOG-KYOON

<a href="#">08415056</a>	<a href="#">5712884</a>	150	03/31/1995	DATA RECEIVING METHOD AND CIRCUIT OF DIGITAL COMMUNICATION SYSTEM	JEONG, DEOG- KYOON
<a href="#">08370904</a>	<a href="#">5621407</a>	150	01/10/1995	DIGITAL/ANALOG CONVERTER	JEONG, DEOG- KYOON
<a href="#">08332561</a>	<a href="#">5574756</a>	150	10/31/1994	METHOD FOR GENERATING DIGITAL COMMUNICATION SYSTEM CLOCK SIGNALS & CIRCUITRY FOR PERFORMING THAT METHOD	JEONG, DEOG- KYOON
<a href="#">08254326</a>	<a href="#">5714904</a>	150	06/06/1994	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG- KYOON

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## Inventor Name Search Result

Your Search was:

Last Name = JEONG

First Name = DEOG-KYOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name 39
<u>60437856</u>	Not Issued	159	01/03/2003	CMOS 3.5 GBPS CONTINUOUS-TIME, LOW-FREQUENCY-GAIN/HIGH-FREQUENCY-BOOSTING JOINT ADAPTATION EQUALIZER AND METHOD ✓	JEONG, DEOG-KYOON
<u>60416017</u>	Not Issued	159	10/04/2002	2.5-10GBPS CMOS TRANSCEIVER WITH ALTERNATING EDGE SAMPLING PHASE DETECTION FOR LOOP CHARACTERISTIC STABILIZATION ✓	JEONG, DEOG-KYOON
<u>60406858</u>	Not Issued	159	08/29/2002	CMOS TRANSCEIVER WITH DUAL CURRENT PATH VCO ✓	JEONG, DEOG-KYOON
<u>60333439</u>	Not Issued	159	11/26/2001	0.6-2.5GBAUD CMOS TRACKED 3X OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION FOR ROBUST CLOCK/DATA RECOVERY ✓	JEONG, DEOG-KYOON
<u>60296652</u>	Not Issued	159	06/06/2001	DATA ENCODING BASED ON TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION ✓	JEONG, DEOG-KYOON
<u>60296213</u>	Not Issued	159	06/05/2001	SCALABLE STORAGE INTERFACE ARCHITECTURE ✓	JEONG, DEOG-KYOON
<u>60252724</u>	Not Issued	159	11/22/2000	METHOD AND APPARATUS FOR STORAGE I/O WITH FULL-DUPLEX ONE-TIME BLOCK I/O TRANSFER AND ADAPTIVE PAYLOAD SIZING ✓	JEONG, DEOG-KYOON
<u>60100057</u>	Not Issued	159	09/10/1998	METHODS AND APPARATUS FOR BIDIRECTIONAL DATA TRANSFER BETWEEN DIGITAL DISPLAY DEVICE AND COMPUTING DEVICES ✓	JEONG, DEOG-KYOON
<u>60082959</u>	Not Issued	159	04/23/1998	SKEW-INSENSITIVE LVDS (LOW VOLTAGE DIFFERENTIAL SWING) RECEIVER ✓	JEONG, DEOG-KYOON
<u>10722842</u>	<u>6876240</u>	150	11/25/2003	WIDE RANGE MULTI-PHASE DELAY-LOCKED LOOP ✓	JEONG, DEOG-KYOON

<u>10356695</u>	<u>6859107</u>	150	01/30/2003	FREQUENCY COMPARATOR WITH HYSTERESIS BETWEEN LOCKED AND UNLOCKED CONDITIONS	JEONG, DEOG-KYOON
<u>10305254</u>	Not Issued	030	11/25/2002	0.6-2.5 GBAUD CMOS TRACKED 3X OVERSAMPLING TRANSCEIVER WITH DEAD ZONE PHASE DETECTION FOR ROBUST CLOCK/DATA RECOVERY ✓	JEONG, DEOG-KYOON
<u>10253534</u>	<u>6781424</u>	150	09/25/2002	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME ✓	JEONG, DEOG-KYOON
<u>10215936</u>	<u>6717468</u>	150	08/08/2002	DYNAMICALLY BIASED FULL-SWING OPERATION AMPLIFIER FOR AN ACTIVE MATRIX LIQUID CRYSTAL DISPLAY DRIVER ✓	JEONG, DEOG-KYOON
<u>10196479</u>	<u>6756828</u>	150	07/17/2002	PHASE LOCK LOOP (PLL) APPARATUS AND METHOD ✓	JEONG, DEOG-KYOON
<u>10183974</u>	Not Issued	094	06/25/2002	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	JEONG, DEOG-KYOON
<u>10045600</u>	<u>6771192</u>	150	11/07/2001	METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER ✓	JEONG, DEOG-KYOON
<u>10037168</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR PLESIOSYNCHRONOUS COMMUNICATIONS WITH NULL INSERTION AND REMOVAL ✓	JEONG, DEOG-KYOON
<u>10036794</u>	Not Issued	090	11/07/2001	METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS ✓	JEONG, DEOG-KYOON
<u>10036135</u>	Not Issued	030	11/07/2001	METHOD AND SYSTEM FOR PACKET ORDERING BASED ON PACKET TYPE ✓	JEONG, DEOG-KYOON
<u>10035591</u>	Not Issued	030	11/07/2001	COMMUNICATIONS ARCHITECTURE FOR STORAGE-BASED DEVICES ✓	JEONG, DEOG-KYOON
<u>09985897</u>	<u>6512408</u>	150	11/06/2001	MIXER STRUCTURE AND METHOD FOR USING SAME ✓	JEONG, DEOG-KYOON
<u>09948123</u>	Not Issued	164	09/05/2001	IMPLEMENTING AN OVERSAMPLING TRANSCEIVER WITH DEAD-ZONE PHASE DETECTION ✓	JEONG, DEOG-KYOON
<u>09943029</u>	Not Issued	071	08/29/2001	DATA RECOVERY USING DATA EYE TRACKING ✓	JEONG, DEOG-KYOON
<u>09897975</u>	<u>6510185</u>	150	07/05/2001	SINGLE CHIP CMOS TRANSMITTER/RECEIVER	JEONG, DEOG-KYOON
<u>09814256</u>	<u>6587525</u>	150	03/21/2001	SYSTEM AND METHOD FOR HIGH-SPEED, SYNCHRONIZED DATA COMMUNICATION	JEONG, DEOG-KYOON

<u>09693516</u>	<u>6462624</u>	150	10/20/2000	HIGH-SPEED AND HIGH- PRECISION PHASE LOCKED LOOP ✓	JEONG, DEOG- KYOON
<u>09234777</u>	<u>6600771</u>	150	01/20/1999	SPREAD SPECTRUM PHASE MODULATION FOR SUPPRESSION OF ELECTROMAGNETIC INTERFERENCE IN PARALLEL DATA CHANNELS ✓	JEONG, DEOG- KYOON
<u>09187559</u>	<u>6151334</u>	150	11/04/1998	SYSTEM AND METHOD FOR SENDING MULTIPLE DATA SIGNALS OVER A SERIAL LINK	JEONG, DEOG- KYOON
<u>09148815</u>	<u>6144242</u>	150	09/04/1998	CONTROLLABLE DELAYS IN MULTIPLE SYNCHRONIZED SIGNALS FOR REDUCED ELECTROMAGNETIC INTERFERENCE AT PEAK FREQUENCIES ✓	JEONG, DEOG- KYOON
<u>09148583</u>	<u>6271816</u>	150	09/04/1998	POWER SAVING CIRCUIT AND METHOD FOR DRIVING AN ACTIVE MATRIX DISPLAY ✓	JEONG, DEOG- KYOON
<u>09146818</u>	<u>6229859</u>	150	09/04/1998	SYSTEM AND METHOD FOR HIGH- SPEED, SYNCHRONIZED DATA COMMUNICATION ✓	JEONG, DEOG- KYOON
<u>09098266</u>	<u>6157263</u>	150	06/16/1998	HIGH-SPEED AND HIGH- PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	JEONG, DEOG- KYOON
<u>09017758</u>	<u>6107946</u>	150	02/03/1998	HIGH SPEED SERIAL LINK FOR FULLY DUPLEXED DATA COMMUNICATION	JEONG, DEOG- KYOON
<u>09013679</u>	<u>6211714</u>	150	01/26/1998	PARALLEL CONDUCTOR SYSTEM FOR REDUCING NOISE IN TRANSMITTING CLOCK SIGNALS	JEONG, DEOG- KYOON
<u>08937262</u>	<u>6100868</u>	150	09/15/1997	HIGH DENSITY COLUMN DRIVERS FOR AN ACTIVE MATRIX DISPLAY ✓	JEONG, DEOG- KYOON
<u>08920336</u>	<u>5955929</u>	150	08/27/1997	VOLTAGE-CONTROLLED OSCILLATOR RESISTANT TO SUPPLY VOLTAGE NOISE ✓	JEONG, DEOG- KYOON
<u>08000430</u>	<u>5332934</u>	150	01/04/1993	SMALL TO FULL SWING CONVERSION CIRCUIT ✓	JEONG, DEOG- KYOON

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